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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,984	12/11/2003	Hui-Min Mao	10113311	2073
34283	7590	07/13/2005	EXAMINER	
QUINTERO LAW OFFICE 1617 BROADWAY, 3RD FLOOR SANTA MONICA, CA 90404			MONDT, JOHANNES P	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/733,984

Applicant(s)

MAO ET AL.

Examiner

Johannes P. Mondt

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 04 May 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) 1-22 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 23-25 is/are rejected.
- 7) ☒ Claim(s) 26 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election without traverse of the Group II invention (claims 23-26 drawn to a structure for a bitline contact hole) in the reply filed on 5/4/05 is acknowledged. Accordingly the claims 1-22 drawn to a method of forming a structure for a bitline contact hole are herewith being withdrawn from consideration.

### *Claim Objections*

2. **Claims 23-26** are objected to because of the following informalities: the wording "and a doped region" (line 6) should be replaced by: "and comprising a doped region". Appropriate correction is required.
3. **Claims 23-26** are objected to because of the following informalities: the wording "and the passivation"" (line 16 of page15 within claim 23) should be replaced by: "and the passivation layer". Appropriate correction is required.
4. **Claim 24** is objected to because of the following informalities: the wording "of the polysilicon" (line 2) should be replaced by: "of the polysilicon layer". Appropriate correction is required.
5. **Claim 25** is objected to because of the following informalities: the wording "of the passivation" (line 2) should be replaced by: "of the passivation layer". Appropriate correction is required.
6. **Claim 26** objected to because of the following informalities: the wording "of the passivation" should be replaced by: "of the passivation layer". Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. **Claim 23** is rejected under 35 U.S.C. 102(b) as being anticipated by Murai (5,410,183). Murai teaches a structure for a bit line contact hole (title, abstract, “Background of the Invention and Figure 1E) comprising: a substrate 1 (col. 4, l. 4); a transistor (defined by gate electrode 23 and source/drain regions 24 and the interposed channel region of the substrate), disposed on the substrate (Figure 1E), comprising a gate layer 23 (loc.cit.) covered by a first insulating layer 2 (col. 4, l. 31), and (comprising) a doped region 24 (loc.cit.) (N.B.: in view of the Specification the only possible interpretation of the claim language is as recited here since the gate layer is not covered by a doped region as an entity separate from other claimed components or elements in Applicant’s disclosure); an inner landing pad (horizontal bottom portion of 5 (col. 4, l. 48-57) disposed on the doped region and parts of the transistor (namely on the drain region and gate oxide film 22 (col. 4, l. 25) and comprising a polysilicon layer 5 (loc.cit.); a passivation layer 2 disposed on the inner landing pad (col. 4, l. 24-29), the transistor and the substrate (Figure 1E); a second insulating layer 4 (col. 4, l. 42-47) disposed on the passivation layer, having a flat surface on the passivation layer (upper surface thereof is both flat and on the passivation layer); a contact plug 9 (col. 5, l. 27-43) disposed on the second insulating layer and the passivation layer (Figure 1E),

electrically connected with the inner landing pad through a contiguous extension of polysilicon 5 (Figure 1E and loc.cit. for element 5); and an interconnected landing pad 8 (col. 5, l. 27-43), deposited on the contact plug (the disclosure only defines the interconnected landing pad as a contiguous but anvil-type addendum to the contact plug, which is exactly the situation in the prior art as cited here).

***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. **Claim 24** is rejected under 35 U.S.C. 103(a) as being unpatentable over Murai (5,410,183) in view of Wu et al (5,786,250). As detailed above, Murai anticipates claim 23. Murai does not necessarily teach the further limitation defined by claim 24, instead teaching the range 500 – 2000 Å, which fails to overlap with the claimed range by about 100 Å or about 20%. However, it would have been obvious to include said further limitation in view of Wu et al, who in a patent on a MOS DRAM structure, hence closely related to Murai, teach a polysilicon landing pad 26 to have a thickness in the range between 50 to 600 Å (col. 6, l. 41-55), thus being as thin as possible in order to cut down on cost of manufacturing the inner landing pad (see Wu et al, col. 3, l. 44-50) while being thick enough to compensate for non-uniformity in etching (loc.cit.). Applicant is reminded that a *prima facie* case of obviousness typically exists when the ranges as claimed overlap the ranges disclosed in the prior art or when the ranges as claimed do

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not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003). In the underlying case the ranges do overlap. *Motivation* to include the teaching by Wu et al in the invention by Murai at least derives from the cost saving on the fabrication of the landing pad within the constraint of its functionality.

11. **Claim 25** is rejected under 35 U.S.C. 103(a) as being unpatentable over Murai (5,410,183) in view of Yeh (6,100,569). As detailed above, Murai anticipates claim 23. Murai does not necessarily teach the further limitation defined by claim 25. However, it would have been obvious to include said further limitation in view of Yeh, who, in a patent on a semiconductor random access memory device with contact (title, abstract), hence closely related to Murai, teaches the selection of silicon nitride for the first-level dielectric layer covering the transistor gate and doped drain region, which corresponds to the passivation layer 2 in Murai (see Yeh, col. 3, l. 23-31). Applicant is reminded that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

#### ***Allowable Subject Matter***

12. **Claim 26** is objected to both for minor informalities (see Claim Objections made above) and for being dependent upon a rejected base claim, but would be allowable if the grounds for said claim objections were removed by amendment and the claim be rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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13. The following is a statement of reasons for the indication of allowable subject matter: the thickness of passivation layer 2 in Murai is significantly greater (2000-8000 Å), and while silicon nitride liners are known in the art of semiconductor memory devices with contact plugs as witnessed by Tanaka et al (6,733,547 B1) said silicon nitride liner by Tanaka et al is not disposed on the landing pad, in contrast with the invention as claimed and as disclosed (see page 7 and Figure 1I: passivation layer 122 is disposed on inner landing pad 112a) thus serving its passivation function also for the polysilicon in inner landing pad 112a.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM

July 10, 2005

Patent Examiner:

A handwritten signature in black ink, appearing to read 'J. Mondt', is written over the printed name.

Johannes Mondt (Art Unit: 2826).